

十一、研究計畫中英文摘要：請就本計畫要點作一概述，並依本計畫性質自訂關鍵詞。

(二) 計畫英文摘要。(五百字以內)

This project plans to combine the “Static Timing Analysis” (STA) and “Formal Verification” techniques, and proposes a novel “Formal Static Timing Analysis” algorithm. Similar to STA, we do not require the user to provide input test patterns. Instead, we try to embed the formal verification engine in the timing analysis routine such that it can efficiently search through all the functional space, enumerate all the possible input patterns, and come up with the closest possible delay analysis.

We lay up our project execution with three milestones in as many years. The focus of our first year will be integrating the functional and timing analysis models. With this integrated model, we can share the analysis data between these two engines, helping each other in finding the most accurate delay value. In the second year, we will finish the FSTA prototype system and also port it to various stages in the design flow, for example, front-end synthesis, place and route, etc, so that we can apply this technique in different areas. In the third year, we will consider adding the deep submicron interconnection effects, for example, signal integrity and statistical timing model, into our FSTA algorithm. We will also consider the possibility of applying our technique to different Electronic Design Automation areas like Power Analysis and Design for Manufacturability, etc.

In summary, our FSTA algorithm will integrate the state-of-the-art techniques from timing analysis and formal verification. We will try to strike the balance between the accuracy and efficiency, and provide a more robust timing analysis technique.