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思源科技—台灣大學合作研究計畫

正規驗證輔助電路最佳化 (II)

Formal-Assisted Technology Dependent Logic Optimization (Phase II)

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一、 Project Description

In the Phase I project, we implemented a SAT-controlled Redundancy Addition and Removal (SatRAR) engine and proposed a Formal Assisted Buffer Insertion (FABI) technique. The SatRAR engine is superior to the previous RAR algorithms because it can identify more alternative logic especially on the hard-to-replace wires. The FABI technique, although not as efficient as the traditional dynamic programming based approaches, can further improve the circuit delay after the traditional ones are performed.

In this Phase II project, we will continue the research on the technology-dependent logic optimization problems. Our focuses will be on (1) SatRAR-based incremental optimization, and (2) Multi-Corner Multi-Mode (MCMM) timing analysis and optimization.

For (1), we will incorporate the physical layout information into our SatRAR data base. The actual cell locations, wire lengths, cell types, and spare cell availabilities will be considered when identifying the alternative logic. In addition, to avoid being stuck at local optima, we will also extend the SatRAR algorithm to the multiple wire/gate addition and removal (MRAR) technique.

The MCMM timing analysis and optimization, on the other hand, is an emerging research and product direction in recent years. Many EDA vendors have proposed solutions and implemented them into their timing analysis and signal integrality tools. For example, Mentor Graphics' Olympus-SoC™ P&R tool, Magama's Blast Fusion® QT, Synopsys' IC Compiler, Cadence's SoC Encounter, ExtremeDA's GoldTime™ Sign-off TA, and CLKWorks' Clock Design Suite, have all addressed the MCMM issues in their featuring products. From the publicly available marketing documents and technical white papers, we know that most of these solutions are based on parallel computing techniques where timing constraints at different modes and corners are considered concurrently. Although these solutions are successful in reducing runtime, however, they may consume about the same *computing resource*, if not more, because the efforts in performing analysis and optimization on individual modes are not reduced by the parallel computing. In this proposal, we will investigate on the "learning technique" by formal verification engines so that the timing analysis on one mode can help the computation on the other modes.

The research on the MCMM timing analysis/optimization problems in academia, however, is not as active as in industry. In [1][2], the authors modeled the MCMM timing effects as a linear hyperplane. Through the hyperplane propagation on the circuit, they can compute the worst case timing in a single path. Although their results did show some performance improvement on the MCMM timing analysis, their approach would inevitably lead to certain inaccuracy due to the over approximation of the hyperplane propagation.

In this proposal, we would like to develop an analytical model for the MCMM timing analysis and optimization problems such that the causal effects between different modes and corners can be characterized by formal engines. We will then apply the formal techniques for the more accurate timing and obtain the better optimized results.

[1] Sari Onaissi and Farid N. Najm, “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners”, in Proc. ICCAD, 2006.

[2] Sari Onaissi and Farid N. Najm, “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners”, in IEEE Trans. CAD, vol. 27, no. 7, July 2008.