

十一、研究計畫中英文摘要：請就本計畫要點作一概述，並依本計畫性質自訂關鍵詞。

(一) 計畫英文摘要。(五百字以內)

Keywords: Trillion-Transistor-Scale System-on-Chip, Simulation, Formal verification, System-level design

As the design complexity keeps increasing, many statistics show that “design verification” has become the most time-consuming step in the modern design flow. Therefore, in order to overcome the future Trillion-Transistor-Scale System-on-Chip (TS SoC) design challenges, innovated and efficient design verification methodology will be the most critical factor.

Simulation is by far the most popular approach in design verification. However, the complexity of simulation is in theory exponential to the size of the design. As a result, the verification gap between test complexity and simulation performance is becoming a very critical problem in the modern design flow.

Formal verification, on the other hand, converts the design into a formal logic model and uses logic and mathematical methods to check if this model has certain specified attributes (called “properties”). In theory it should be much more powerful than the simulation engine in exploring the design space. However, with the rapid increase in the design complexity, the improvement in formal verification still cannot catch up with the advance in circuit design.

Therefore, we propose to examine the advantages and disadvantages of both techniques and figure out the reasons that cause the differences. We plan to implement a combined simulation and formal verification framework that can serve as a robust and efficient verification tool in the system-level design flow.